**SYLLABUS**[1]

1. **Information about the Program**

| | |
|---|---|
| 1.1 Higher education institution | Politehnica University of Timişoara |
| 1.2 Faculty[2] / Department[3] | Automation and Computers/ Computers |
| 1.3 Chair | - |
| 1.4 Domain of study | Computers and Information Technology |
| 1.5 Study level | Bachelor |
| 1.6 Study programme / Qualification | Computers / engineer |

**2. Information about the Course**

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|---|---|---|---|---|---|---|---|
| 2.1 Course | | | Digital Logic | | | | |
| 2.2 Lecturer | | | Conf. dr. ing. Doru Todinca | | | | |
| 2.3 Academic staff for seminars/labs | | | Conf. dr. ing. Doru Todinca | | | | |
| 2.4 Study year | 1 | 2.5 Semester | 2 | 2.6 Assessment type | E | 2.7 Course type | Mandatory |

**3. Total time estimated** (hours/ semester of didactical activities)

| | | | | | | |
|---|---|---|---|---|---|---|
| 3.1 Hours / week | 4 | of which: | 3.2 lecture hours | 2 | 3.3 seminar/lab hours | 2 |
| 3.4 Total curriculum hours | 56 | of which: | 3.5 lecture hours | 28 | 3.6 seminar/lab hours | 28 |
| Time distribution | | | | | | hours |
| Study using manuals, support materials, bibliography and notes | | | | | | 20 |
| Supplementary documentation in library, speciality electronic platforms and on site | | | | | | 20 |
| Supplementary preparation for seminars/labs, homeworks, reviews, portofolios and essays | | | | | | 21 |
| Tutoring activities | | | | | | 7 |
| Exams | | | | | | 3 |
| Other | | | | | | |

| | |
|---|---|
| **3.7 Total - hours of individual study** | 61 |
| **3.8 Total - hours per semester** | 66 |
| a. **Credits** | 5 |

**4. Prerequisites** (if appropriate)

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|---|---|
| 4.1 curriculum | • Algebra, Computer programming |
| 4.2 competencies | • Operarea cu fundamente ştiinţifice, inginereşti şi ale informaticii |

**5. Conditions** (if appropriate)

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|---|---|
| 5.1 for lectures | • Big classroom. Materials: laptop, whiteboard, projector |
| 5.2 for seminars/labs | • 15-20 PCs, OMNeT++ and VHDL, whiteboard |

1 Formularul corespunde Fişei Disciplinei promovată prin OMECTS 5703/18.12.2011 (Anexa3);

2 Se înscrie numele facultăţii care gestionează programul de studiu căruia îi aparţine disciplina;

3 Se înscrie numele departamentului căruia i-a fost încredinţată susţinerea disciplinei şi de care aparţine titularul cursului;

## 6. Specific competencies acquired

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|---|---|
| Professional competencies[4] | • Operarea cu fundamente ştiinţifice, inginereşti şi ale informaticii<br>• Proiectarea componentelor hardware, software şi de comunicaţii<br>• Soluţionarea problemelor folosind instrumentele ştiinţei şi ingineriei calculatoarelor<br>• Îmbunătăţirea performanţelor sistemelor hardware, software şi de comunicaţii |
| Transversal competencies | • Comportarea onorabilă, responsabilă, etică, în spiritul legii pentru a asigura rezolvarea problemei<br>• Identificarea, descrierea și derularea proceselor din managementul proiectelor, cu preluarea diferitelor roluri în echipă și descrierea clară și concisă, verbal și în scris, în limba română și într-o limbă de circulație internațională, a domeniului de activitate<br>• Demonstarea spiritului de iniţiativă şi acţiune pentru actualizarea cunoştinţelor profesionale, economice şi de cultură organizaţională |

## 7. Objectives of the course (issued from the list of the comptenecies acquired)

| | |
|---|---|
| 7.1 Aim | • To acquire basic notions about boolean algebra, combinational and sequential circuits and their design |
| 7.2 Specific objectives | • To be familiar with boolean algebra axioms and theorems. To design comhinational circuits using different minimization techniques. To understand sequential logic. To be able to design counters, registers and, in general, sequential state machines. |

## 8. Content

| 8.1 Lecture | Hours | Instruction methods |
|---|---|---|
| 1Intdoduction<br>1.1. Number representation.<br>1.2 Signals. | 2 | Slide-based presentations, discutions, examples. |
| 2Boolean algebra<br>2.1. Logic functions. Truth tables<br>2.2 Axioms and theorems of boolean algebra. De Morgan's laws. | 4 | |
| 3. Combintaorial circuits.<br>3,1 Using truth tables for boolean functions representation.<br>3.2 Combinational circuits minimizations. Karnaugh maps.<br>3.3. Don't care input combinations<br>3.4. Timing hazards. Static and dynamic hazards. | 4 | |
| **4.** Basic notions of VHDL<br>4.1. Entities and architecture.<br>4.2. Notions of structural modeling in VHDL. | 4 | |
| 5. Combinational circuits design<br>5.1. Designing decoders and encoders. | 4 | |

[4] Aspectul competenţelor profesionale va fi tratat cf. Metodologiei OMECTS 5703/18.12.2011. Se vor prelua competenţele care sunt precizate în Registrul Naţional al Calificărilor din Învăţământul Superior RNCIS (http://www.rncis.ro/portal/page?_pageid=117,70218&_dad=portal&_schema=PORTAL) pentru domeniul de studiu de la pct. 1.4 şi programul de studii de la pct. 1.6 din această fişă.

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|---|---|---|
| 5.2. Designing multiplexers and demultiplexers<br>5.3. Comparators.<br>5.4. Binary adders, subtracters and ALUs | | |
| 6. Basics of sequential logic design<br>6.1. Latches and flip-flops. The S-R latch<br>6.2 S-R latch with enable. The D latch<br>6.3. Edge triggered D flip-flop<br>6.4. Master-slave flip-flops. J-K master slave flip-flop. T flip-flop | 4 | |
| 7 State machines<br>7.1. State machine structure. Output logicMealy and Moore state machines.<br>7.2. State machines design. Characteristic equations<br>7.3. Analysis of state machines wirh D flip-flops<br>7.4. Analysis of state machine with J-K flip-flops<br>7.5. State minimization. Counters and shift registers<br>7.6 Designing state machines using state diagrams.<br>7.7 Designing state machines using transition lists | 6 | |
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References


1. **J. F. Wakerly. Digital Design: Principles and Practices (4th Edition). Prentice Hall, 2005**
2. P. Eles, K Kuchcinski, Z. Peng: *System Synthesis with VHDL*, Kluwer Academic, 1997.
3. W. Stallings, Data and Computer Communications, Eight Edition,Pearson Prentice Hall, 2007


| 8.2 Seminar/lab | Hours | Instruction methods |
|---|---|---|
| 1. Number representation. Exercices | 2 | Short presentation, discutions, implementation |
| 2. Logical gates. Truth tables. Boolean equations | 4 | |
| 3. VHDL simulations of simple circuits | 4 | |
| 4. Combinational logic. Design and simulation of combinational circuits | 6 | |
| 5. VHDL simulation of latches and flip-flops. | 6 | |
| 6. Design and simulation of sequential logic (counters, shift registers, state machines). | 6 | |
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References


1. 1. **J. F. Wakerly. Digital Design: Principles and Practices (4th Edition). Prentice Hall, 2005**
2. P. Eles, K Kuchcinski, Z. Peng: *System Synthesis with VHDL*, Kluwer Academic, 1997.
3. P. Ashenden, The VHDL Cookbook, 2011


**9. Correlation between the course content and the requirements of the specialists in the field and the expectations of the main employers**

- Digital logic is the fundament of students' future knowledge in hardware desing.

**10. Assessment**

| Activity type | 10.1 Assessment criteria | 10.2 Assessment methods | 10.3 Weight in final mark |
|---|---|---|---|
| 10.4 Lecture | Answers to questions related to the content of the lectures | Written exam | 50% |
| 10.5 Seminar /labs | Solving the problems given during the labs | Describing the proposed solution, answerinq questions | 20% |
| | Homeworks (assignments) | Describing the proposed solution, answerinq questions | 20% |
| | Presence | Presence monitoring | 10% |
| 10.6 Minimal performance standards (minimal specific knowledge required for passing the exam, the means to assess mastering the specific knowledge) | | | |
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11. **International compatibility**

1 Carnegie Mellon University. Structure and Design of Digital Systems, ECE 18-240

2. University of Michigan, Logic Circuit Synthesis and Optimization, EECS 478

3. University of California Berkeley. Components and Design Techniques for Digital Systems, CS 150

| Date | Signature of the course instructor | Signatures of the academic staff for seminars/labs |
|---|---|---|
| | Conf. dr. ing. Doru Todinca | Conf. dr. ing. Doru Todinca |
| | …… | …… |

Date of approval in the Department

Signature of the Department Director

Prof. dr. Ing. Vladimir Ioan CREŢU

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